CLAIMS

1. A method of forming a transistor gate, comprising:

forming one or more conductive materials over a semiconductor substrate:

forming a block over the one or more conductive materials; the block comprising a photoresist mass and a material other than photoresist which is against the photoresist; and

transferring a pattern from the block to the one or more conductive materials to pattern a transistor gate construction from the one or more conductive materials.

- 2. The method of claim 1 further comprising removing the block from over the transistor gate construction.
- 3. The method of claim 1 further comprising defining a channel region within the semiconductor substrate beneath the transistor gate construction; and forming source/drain regions within the semiconductor substrate and spaced from one another by the channel region.
- 4. The method of claim 1 wherein the photoresist releases an acid, and wherein the material other than photoresist is a coating which cross-links when exposed to the acid from the photoresist.

- 5. The method of claim 1 wherein the material other than photoresist corresponds to a material designated as AZ R200™ by Clariant International, Ltd.
- 6. The method of claim 1 wherein the one or more conductive materials comprise conductively doped silicon.
 - 7. A method of forming a transistor gate, comprising:

forming one or more conductive materials over a semiconductor substrate;

forming a patterned photoresist block over the one or more conductive materials; the photoresist block covering a first portion of the one or more conductive materials and leaving a second portion of the one or more conductive materials uncovered;

forming a coating over the patterned photoresist block and over at least some of the second portion of the one or more conductive materials;

selectively removing the coating from over the second portion of the one or more conductive materials while leaving the coating on the photoresist block; the photoresist block and coating remaining on the photoresist block together defining a masking block that is laterally wider than the photoresist block; and

transferring a pattern from the masking block to the one or more conductive materials to pattern a transistor gate construction from the one or more conductive materials.

- 8. The method of claim 7 further comprising removing the masking block from over the transistor gate construction.
- 9. The method of claim 7 further comprising defining a channel region within the semiconductor substrate beneath the transistor gate construction; and forming source/drain regions within the semiconductor substrate and spaced from one another by the channel region.
- 10. The method of claim 7 wherein the photoresist releases an acid, and wherein the coating forms cross-links when exposed to the acid from the photoresist.
- 11. The method of claim 7 wherein the material other than photoresist corresponds to a material designated as AZ R200™ by Clariant International, Ltd.

12. A method of forming a programmable read-only memory construction, comprising:

forming one or more conductive materials over a semiconductor substrate;

forming a block over the one or more conductive materials; the block comprising a photoresist mass and a material other than photoresist which is against the photoresist;

transferring a pattern from the block to the one or more conductive materials to pattern a floating gate construction from the one or more conductive materials:

forming a dielectric material over the floating gate construction; and forming a control gate over the dielectric material.

- 13. The method of claim 12 further comprising defining a channel region within the semiconductor substrate beneath the floating gate construction; and forming source/drain regions within the semiconductor substrate and spaced from one another by the channel region.
- 14. The method of claim 12 wherein the one or more conductive materials comprise conductively doped silicon.
- 15. The method of claim 12 wherein the photoresist releases an acid, and wherein the material other than photoresist is a coating which cross-links when exposed to the acid from the photoresist.

- 16. The method of claim 12 wherein the material other than photoresist corresponds to a material designated as AZ R200™ by Clariant International, Ltd.
- 17. The method of claim 12 wherein the control gate, dielectric material and floating gate are incorporated into a FLASH memory device.

18. A method of forming at least two programmable read-only memory constructions, comprising:

forming at least one conductive material over a semiconductor substrate;

forming at least two patterned photoresist blocks over the conductive material; a pair of adjacent photoresist blocks being separated by a first gap;

forming a coating over the pair of adjacent photoresist blocks and across the first gap between the adjacent blocks;

selectively removing the coating from across the first gap while leaving the coating on the pair of adjacent photoresist blocks; the pair of photoresist blocks and coating remaining on the pair of photoresist blocks together defining a pair of masking blocks that are separated by a second gap; the second gap being narrower than the first gap;

transferring a pattern from the masking blocks to the conductive material to pattern a pair of spaced floating gate constructions from the conductive material;

. forming a dielectric material over the spaced floating gate constructions; and

forming control gate material over the dielectric material.

19. The method of claim 18 wherein the photoresist releases an acid, and wherein the coating comprises a material which cross-links when exposed to the acid from the photoresist.

- 20. The method of claim 18 wherein the coating corresponds to a material designated as AZ R200™ by Clariant International, Ltd.
- 21. The method of claim 18 wherein the control gate material, dielectric material and floating gates are incorporated into a pair of FLASH memory devices.
- 22. The method of claim 18 wherein the patterned photoresist blocks are formed by a photolithographic process; wherein the photolithographic process is limited to a minimum feature size that can be obtained by the photolithographic process; and wherein a distance between the spaced floating gate constructions is less than said minimum feature size.
- 23. The method of claim 22 wherein the first gap corresponds to about said minimum feature size.